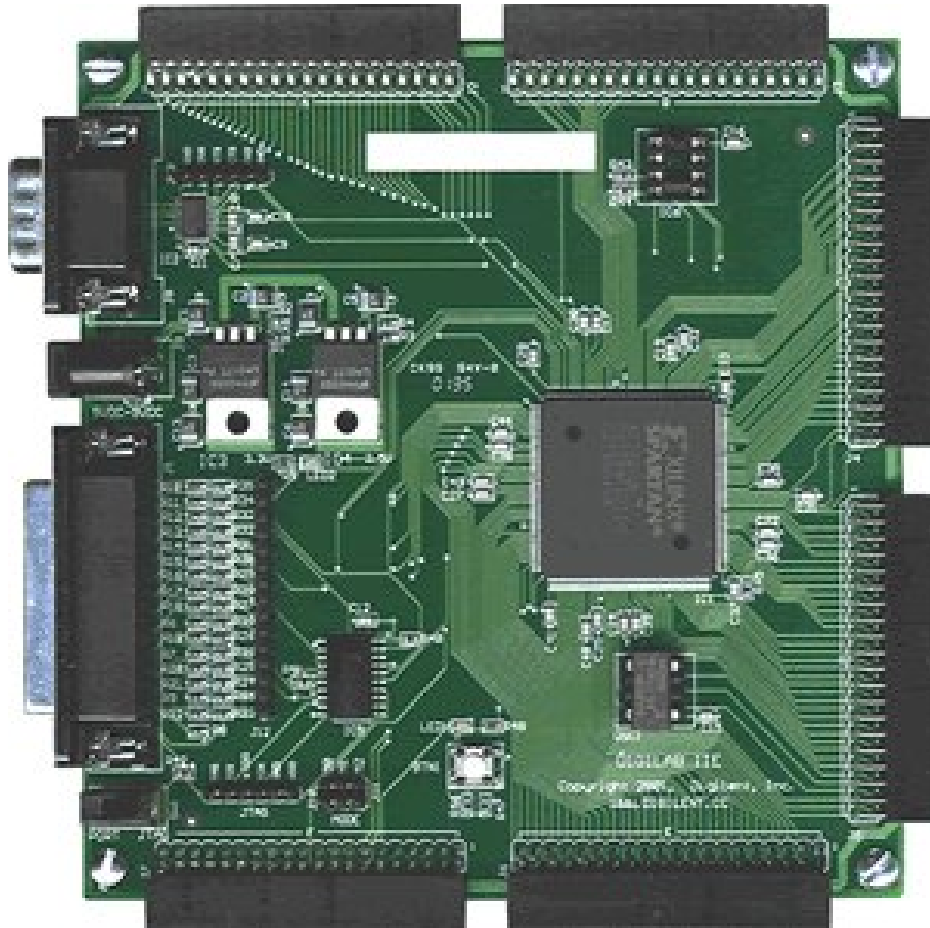# Xilinx Spartan IIE

And Prototyping Board,

Operations Handbook

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### SCIPP Intern 2006

Contents:

Hardware

Signal Source:

This software was designed by Kunal Arya and given to the 2005 Interns. The software was written to run the Muon Lifetime Experiment. The project relies on a clean source out of well-tuned Scintillator Panels. The more accurately the panels are tuned, the finer your results will be. Once you have a clean signal out of the panels, you need to amplify and discriminate the signal. The Xilinx board can only register a digital pulse. There are several different digital standards that the Xilinx can accept most between 2.5 and 4 volts. In most cases the board does not need to be setup for a specific pulse, but if you know the standard, you can specify which to use (Red Arrows).
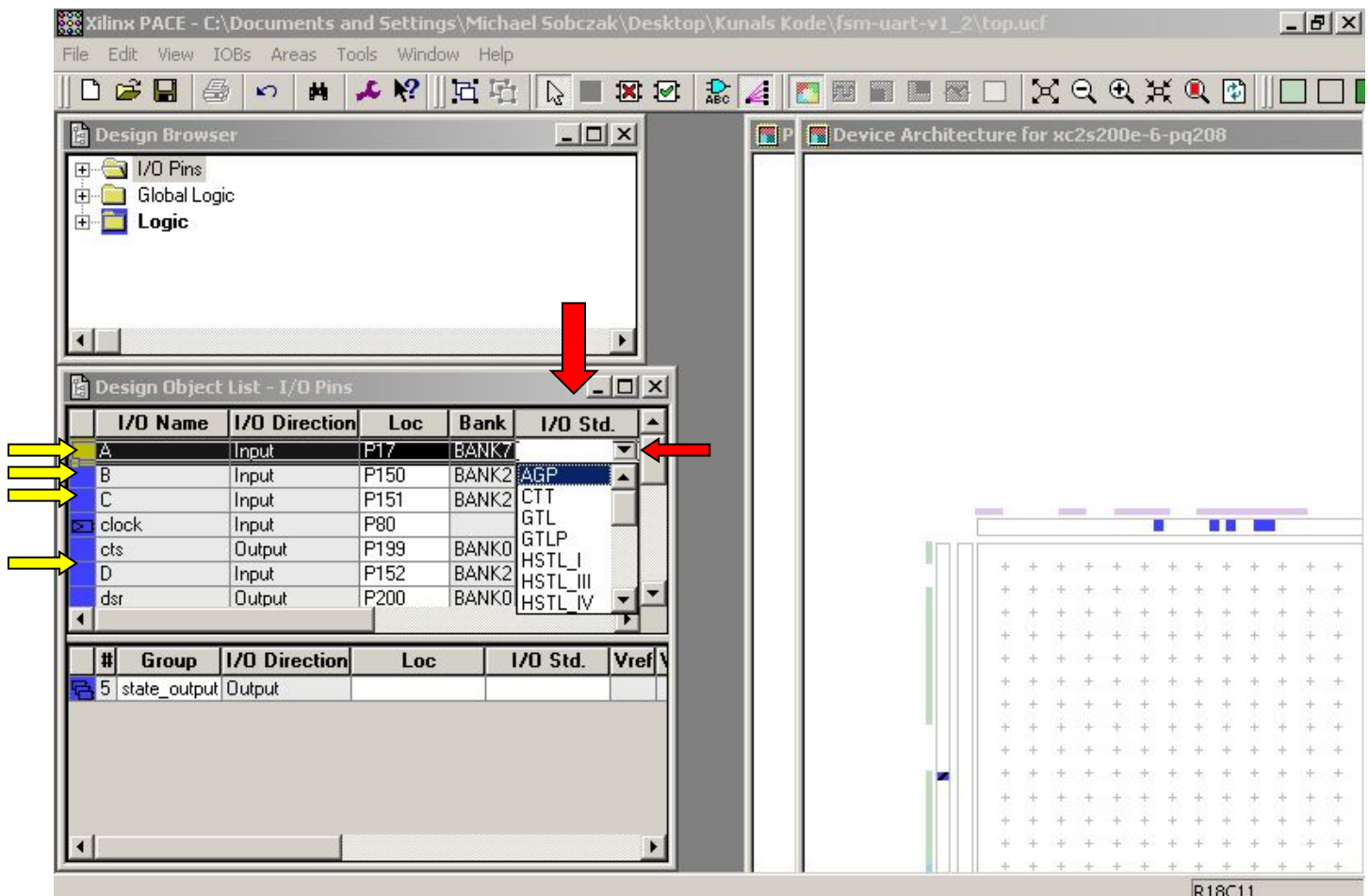
The Signals are collected from Pins Defined in Xilinx ISE 7.1i as "A B C D" (Yellow Arrows)

Signal Amp and Discriminator:

The signals produced by the Scintillator panels are small and vary greatly with the intensity of the Muon passing through. These pulses would cause chaos and confusion within any logic system. The Quarknet 2 DAQ board has an amplifier and discriminator built into the data line. The pulses are amplified by a factor of 10 before being sent to the discriminator.

The discriminator's purpose is to take a pulse out of the scintillator and turn it into a readable square pulse. Very much like this system here:
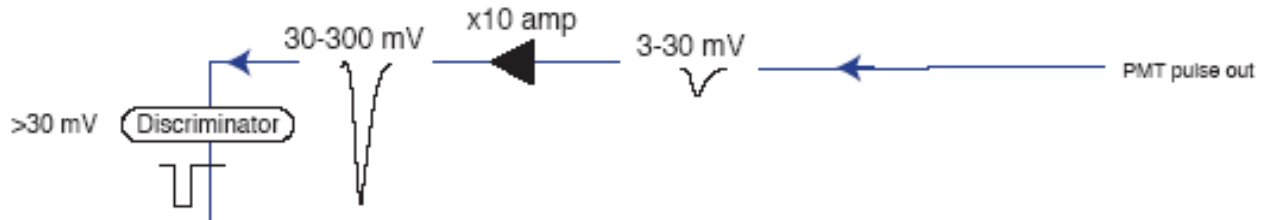
Our application puts out higher voltages, but the concept is the same.

Xilinx Spartan II-200e:

The Xilinx system used during the internship is made of two mated parts. The Xilinx FPGA, a Spartan IIe and a prototyping board made by Digilint. The Xilinx is an FPGA, a Field Programmable Gate Array. It's basically an IC that can be rebuilt without extensive outside support (hence the "Field Programmable" name). This particular model has the ability to accept 120 differential inputs at 19 different voltage standards. We're only using four inputs and probably only one voltage standard, but you get a feeling for how powerful this piece of equipment really is. The Spartan IIe has a clock cycle of 20ns meaning its very easy for us to track the movement of a Muon through the Scintillator Panels connected to the board.

Software

Hyper Terminal (for Quarknet control):

Hyper Terminal is a program typically built into most windows systems. Hyper Term is a program that allows you to communicate and send commands to devices connected through a modem or, in our application, a serial connection. NOTE!!! Wait until Hyper Term is open before powering the Quarknet DAQ!

You can access Hyper Terminal in XP systems by clicking:
Start, All Programs, Accessories, Communications, Hyper Terminal
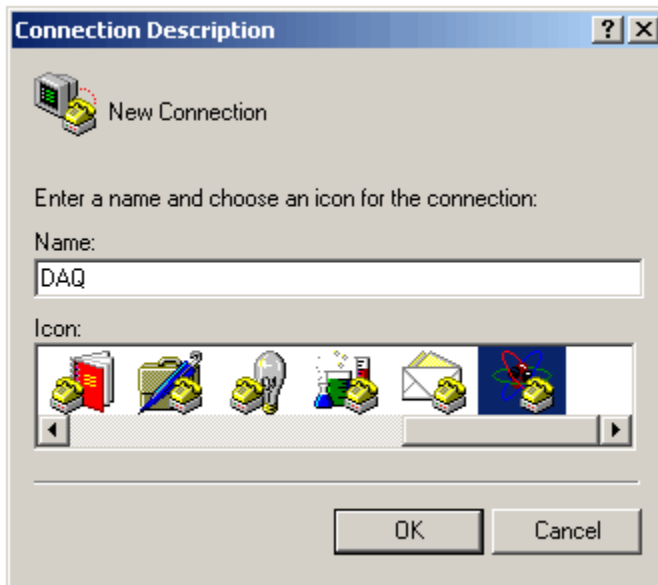
This is the first thing that will appear on Hyper Terminal. The name you use doesn't really mater, however, it should be something you can remember and use later on.

Press ok after you select a name and you will be taken to the connection settings window.

This is the Connection Settings Window.

Here you define where the data is coming from.

On my computer, it's using COM5.

This window shows the settings for your connection (COM 5 or otherwise).

First on the list is Bits per second, also commonly know as the Baud Rate

Next is the Number of Data Bits

Parity Settings

Number of Stop Bits

And Flow Control

The connection to the Quarknet DAQ can be modified once you can communicate with it, but it's default values are:

Baud:	9600
Data Bits:	8
Parity:	None
Stop Bits:	1
Flow Control:	Off

In our use, we found it beneficial to increase the Baud rate to 115000bps to help collect data faster.

For more information of controlling the Quarknet DAQ, Here is a link to their User Guide. It contains the information I listed and a list of the commands the board will accept. It also explains how to set up the collector for different experiments.
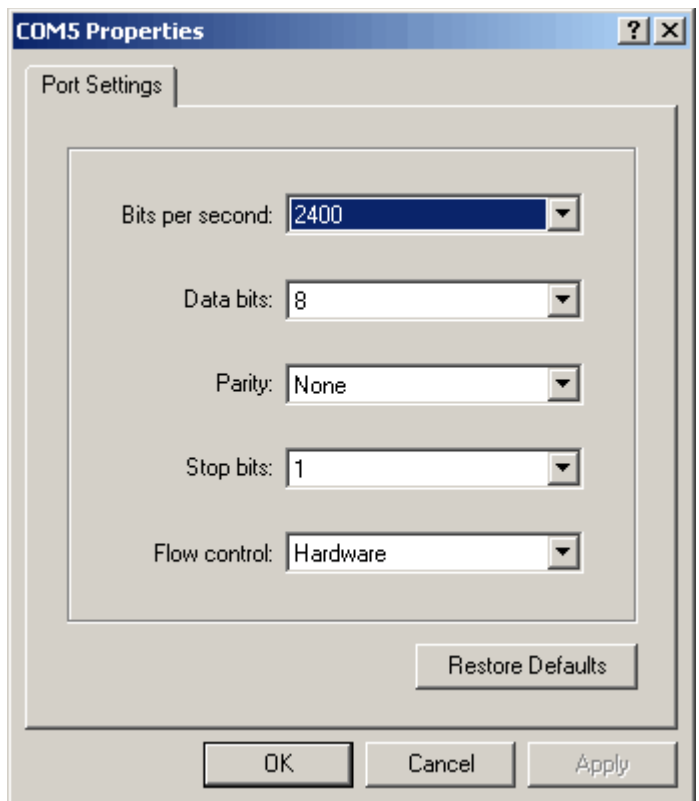
Xilinx ISE 7.1i

The ISE software is used to interface and program the Xilinx FPGA. This program is very advanced, if you have never programmed in something similar to C, I would NOT recommend modifying the code provided by Kunal Arya, a grad student who donated the program to us. The FPGA is a powerful piece of technology that requires clean experienced code to run.

The code provided by Kunal is split up in these files:

- baud.v
- baudrate.v
- datafsm.v
- debouncer.v
- debouncer_tester.v
- fsm-uart-v1_2.ise
- state_machine_tester.v
- top.ucf
- top.v
- top_timesim.v
- uart_tx.v
- uart_tx_tf.v

Here is a link for all the files: (fsm-uart-v1_2.zip)

It may sound like a lot, but every file plays it's part in this code. I personally recommend that you find someone in the lab who has or is working with FPGA systems and get help transferring this program to the Xilinx board.

This file explains how the State Machine program works.

All of Kunal's code is stored here: Muon Code

Please remember, do not modify the code unless you know what your doing. The FPGA is a fragile piece of equipment and mistakes happen quickly.

Muon Lifetime Collector exe:

Kunal also wrote an interface program for the FPGA. This program collects the Muon Lifetime data that has been collected and stores it in a text file. If you import this text data into excel, you can quickly average it and get your Muon Lifetime! The program is simple, just set your baud rate, COM port and Output location and your ready to collect.
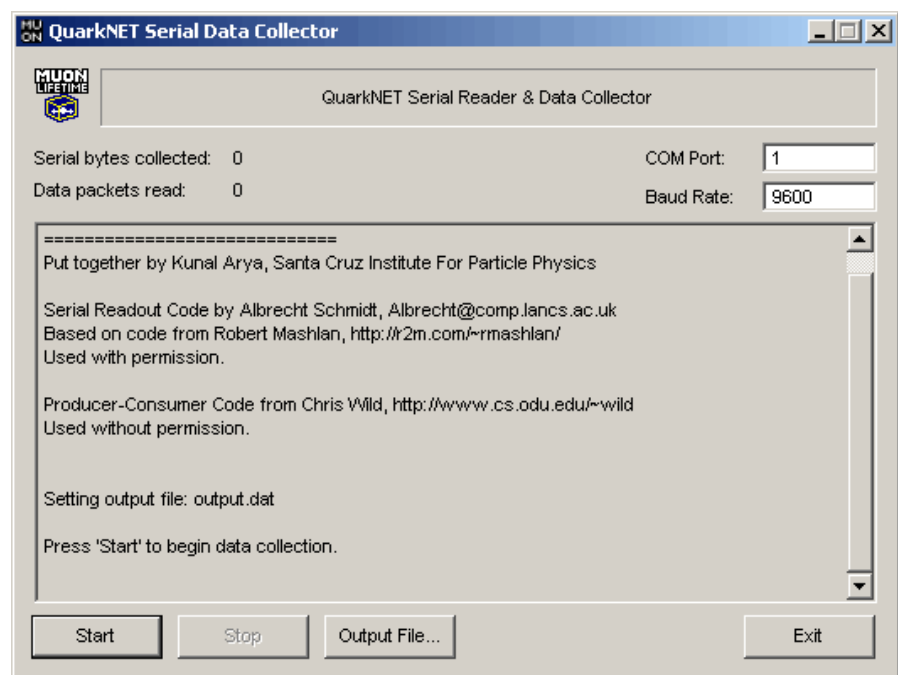
Links:

Xilinx

Digilent Xilinx Proto-board

ISE 7.1i

Kunal's Web Space

Quarknet

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